This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Previously Amended) A method for manufacturing an integrated semiconductor device, having a plurality of connection levels, comprising:

forming a first conductive region inside or above a substrate of semiconductor material;

forming a first insulating region of dielectric material above the first conductive region;

forming a first through region of electrically conductive material inside the first insulating region, and in direct electrical contact with the first conductive region;

forming a second conductive region above the first insulating region, in a position not aligned and not in contact with the first through region;

forming a second insulating region of dielectric material, covering the second conductive region;

forming, inside the second insulating region, a second through region of electrically conductive material, extending as far as the first through region, aligned and in direct electrical contact with the first through region; and

forming, above the second insulating region, a third conductive region aligned and in direct electrical contact with the second through region, wherein the first conductive region is of metal material, a third insulating region extends above the substrate, and the first conductive region extends above the third insulating region.

2. (Original) The method according to claim 1 wherein the first and second through regions have a substantially constant cross-sectional dimension.

3. (Original) The method according to claim 1 wherein the step of forming the first conductive regions comprises the step of introducing doping ion species inside the substrate.

4. (Cancelled) The method according to claim 1 wherein the first conductive region is of metal material, a third insulating region extends above the substrate, and the first conductive region extends above the third insulating region.

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5. (Original) The method according to claim 1 wherein the second and the third conductive regions are formed in successive metal levels.

6. (Original) The method according to claim 1 wherein the first insulating region comprises a first insulating layer of a first dielectric material, and a second insulating layer of a second dielectric material, superimposed on each other, the step of forming the first through region comprises, in succession, the steps of etching the second dielectric material with first etching parameters, etching the first dielectric material with second etching parameters, thereby forming a through aperture in the first insulating region, and filling the through aperture with the electrically conductive material.

7. (Original) The method according to claim 6 wherein the first dielectric material comprises silicon oxide, and the second dielectric material comprises silicon nitride.

8. (Original) A method according to claim 6 wherein the first dielectric material comprises silicon nitride, and the second dielectric material comprises silicon oxide.

9. (Previously Amended) A method of forming an integrated semiconductor structure having a plurality of connection levels, comprising:

forming a first conductive region;

forming a first insulating layer having an upper surface over the first conductive region;

etching a first opening through the first insulating layer to expose a portion of the first conductive region;

forming a first conductive plug that fills the first opening and is electrically coupled to the first conductive region, the first conductive plug having an upper surface extending no further than the upper surface of the first insulating layer;

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forming a second insulating layer having an upper surface over the first insulating layer;

etching a second opening through the second insulating layer to expose a portion of the upper surface of the first conductive plug;

forming a second conductive plug that fills the second opening and is electrically coupled to the first conductive plug, the second conductive plug directly contacting the upper surface of the first conductive plug, and further having an upper surface extending no further than the upper surface of the second insulating layer;

forming a third opening through the first insulating layer;

forming a third conductive plug that fills the third opening and has an upper surface extending no further than the upper surface of the first insulating layer, the first and third conductive plugs being formed simultaneously;

forming a fourth opening through the second insulating layer in a position not directly above the third conductive plug;

forming a fourth conductive plug that fills the fourth opening, second and fourth conductive plugs being formed simultaneously; and

forming a second conductive region over the first insulating layer, the second conductive region directly electrically coupling the third conductive plug to the fourth conductive plug.

10. (Original) The method of claim 9 wherein forming the first conductive region comprises implanting a dopant into a substrate over which the first insulating layer is formed.

11. (Original) The method of claim 9 wherein forming the first conductive region comprises depositing a semiconductor material prior to forming the first insulating layer.

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12. (Original) The method of claim 9 wherein forming the first conductive plug comprises:

depositing a conductive layer over the first insulating layer and filling the first opening; and

removing the conductive layer over the first insulating layer by polishing to leave conductive material filling the first contact via.

13. (Original) The method of claim 9 wherein forming the second insulating layer comprises:

forming a first dielectric layer over the first conductive region; and

forming a second dielectric layer over the first dielectric layer.

14. (Original) The method of claim 13 wherein forming the second opening comprises etching through the second dielectric layer and subsequently etching through the first dielectric layer.

15. (Previously Amended) A method for manufacturing an integrated semiconductor device, having a plurality of connection levels, comprising:

forming a first conductive region inside or above a substrate of semiconductor material;

forming a first insulating region on the first conductive region;

forming a first opening completely through the first insulating region, thereby exposing the first conductive region;

forming a first through region by filling the first opening with electrically conductive material to directly contact the first conductive region;

forming a second insulating region on the first conductive region and the first insulating region;

forming a second opening completely through the second insulating region, thereby exposing the first through region;

forming a second through region by filling the second opening with electrically conductive material to directly contact the first through region;

forming, above the second insulating region, a second conductive region aligned and in direct contact with the second through region; and

forming a third insulating region on the substrate, wherein the first conductive region extends above the third insulating region.

16. (Cancelled) The method according to claim 15, further comprising forming a third insulating region on the substrate, wherein the first conductive region extends above the third insulating region.

17. (Original) The method according to claim 15 wherein the first and second conductive regions are formed in successive metal levels.

18. (Original) The method according to claim 15 wherein the first insulating region comprises a first insulating layer of a first dielectric material, and a second insulating layer of a second dielectric material, superimposed on each other, and the step of forming the first opening comprises selectively etching the second dielectric material with respect to the first dielectric material and then etching the first dielectric material.

19. (Original) The method according to claim 18 wherein the first dielectric material comprises silicon oxide, and the second dielectric material comprises silicon nitride.

20. (Original) A method according to claim 18 wherein the first dielectric material comprises silicon nitride, and the second dielectric material comprises silicon oxide.

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21. (Previously Added) A method for manufacturing an integrated semiconductor device, having a plurality of connection levels, comprising:

forming a first conductive region inside or above a substrate of semiconductor material;

forming a first insulating region of dielectric material above the first conductive region;

forming a first through region of electrically conductive material inside the first insulating region, and in direct electrical contact with the first conductive region;

forming a conductive layer on the first insulating region;

etching the conductive layer to remove all of the conductive layer directly above the first through region and simultaneously form a second conductive region in a position not aligned and not in contact with the first through region;

forming a second insulating region of dielectric material, covering the second conductive region;

forming, inside the second insulating region, a second through region of electrically conductive material, extending as far as the first through region, aligned and in direct electrical contact with the first through region; and

forming, above the second insulating region, a third conductive region aligned and in direct electrical contact with the second through region.

22. (Previously Added) The method according to claim 25, further comprising forming a third insulating region on the substrate, wherein the first conductive region extends above the third insulating region.

23. (Previously Added) The method according to claim 21, further comprising forming an etch stop layer of a first dielectric material on the second conductive region and the first insulating region; wherein the second insulating region is formed of a second dielectric material different than the etch stop layer, and the second through region is formed through the etch stop layer and the second insulating region.

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24. (Previously Added) The method according to claim 21, further comprising:

forming a third through region of electrically conductive material inside the first insulating region and spaced apart from the first through region, the first and third through regions being formed simultaneously;

forming, inside the second insulating region, a fourth through region of electrically conductive material, extending as far as the third through region, aligned and in direct electrical contact with the third through region, the second and fourth through regions being formed simultaneously, wherein the second conductive region is spaced apart from and positioned between the second and fourth through regions.

25. (Previously Added) The method according to claim 21, further comprising:

forming a third through region of electrically conductive material inside the first insulating region and spaced apart from the first through region, the first and third through regions being formed simultaneously;

forming, inside the second insulating region and not directly above the third through region, a fourth through region of electrically conductive material, the second and fourth

through regions being formed simultaneously, wherein the second conductive region directly electrically connects the fourth through region to the third through region.

26. (Previously Added) A method for manufacturing an integrated semiconductor device, having a plurality of connection levels, comprising:

forming a first conductive region inside or above a substrate of semiconductor material;

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forming a first insulating region of dielectric material above the first conductive region;

forming a first through region of electrically conductive material inside the first insulating region, and in direct electrical contact with the first conductive region;

forming a second conductive region above the first insulating region, in a position not aligned and not in contact with the first through region;

forming an etch stop layer of a first dielectric material on the second conductive region and the first insulating region;

forming on the etch stop layer a second insulating region of a second dielectric material different than the etch stop layer;

forming, inside the etch stop layer and the second insulating region, a second through region of electrically conductive material, extending as far as the first through region, aligned and in direct electrical contact with the first through region; and

forming, above the second insulating region, a third conductive region aligned and in direct electrical contact with the second through region.

27. (Previously Added) The method according to claim 28, further comprising forming a third insulating region on the substrate, wherein the first conductive region extends above the third insulating region.

28. (Previously Added) The method according to claim 26, further comprising:

forming a third through region of electrically conductive material inside the first insulating region and spaced apart from the first through region, the first and third through regions being formed simultaneously;

forming, inside the second insulating region, a fourth through region of electrically conductive material, extending as far as the third through region, aligned and in direct electrical contact with the third through region, the second and fourth through regions being formed simultaneously, wherein the second conductive region is spaced apart from and positioned between the second and fourth through regions.

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29. (Previously Added) The method according to claim 26, further comprising:

forming a third through region of electrically conductive material inside the first insulating region and spaced apart from the first through region, the first and third through regions being formed simultaneously;

forming, inside the second insulating region and not directly above the third through region, a fourth through region of electrically conductive material, the second and fourth through regions being formed simultaneously, wherein the second conductive region directly electrically connects the fourth through region to the third through region.

30. (New) A method for manufacturing an integrated semiconductor device, having a plurality of connection levels, comprising:

forming a first conductive region inside or above a substrate of semiconductor material;

forming a first insulating region of dielectric material above the first conductive region;

forming a first through region of electrically conductive material inside the first insulating region, and in direct electrical contact with the first conductive region;

forming a second through region of electrically conductive material inside the first insulating region, the first and second through regions being formed simultaneously;

forming a second conductive region above the first insulating region, in a position between and not in contact with the first and second through regions;

forming a second insulating region of dielectric material, covering the second conductive region;

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forming, through the second insulating region, a third through region of electrically conductive material, extending as far as the first through region, aligned and in direct electrical contact with the first through region; and

forming, through the second insulating region, a fourth conductive region aligned and in direct electrical contact with the second through region, the third and fourth conductive regions being formed simultaneously after forming the second insulating region above the second conductive region.

31. (New) The method according to claim 30, further comprising forming a third insulating region on the substrate, wherein the first conductive region extends above the third insulating region.

32. (New) The method according to claim 30, further comprising forming an etch stop layer of a first dielectric material on the second conductive region and the first insulating region; wherein the second insulating region is formed of a second dielectric material different than the etch stop layer, and the third and fourth through regions are formed through the etch stop layer and the second insulating region.

33. (New) The method according to claim 30 wherein the second insulating region is a single dielectric layer that covers the second conductive region and separates the second conductive region from the third and fourth through regions.